Paper No. 29

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte HIDEMI TAKASU

Appeal No. 1997-3305
Application No. 08/200,312

HEARD: NOVEMBER 16, 2000

Before PAK, WALTZ, and TIERNEY, **Administrative Patent Judges.**

WALTZ, **Administrative Patent Judge.**

DECISION ON APPEAL

This is an appeal under 35 U.S.C. § 134 from the examiner's final rejection of claims 1, 2 and 10 through 12, which are the only claims remaining in this application.

According to appellant, the invention is directed to a process for fabricating semiconductor devices in which a buried layer is formed without producing surface defects or autodoping a layer superimposed on the substrate containing the buried layer (Brief, page 1). Appellant states that claims 2 and 12 fall separately from claim 1 while claims 10 and 11 stand or fall with

claim 2 (Brief, page 4). Furthermore, appellant presents specific, substantive reasons for the separate patentability of claims 1, 2 and 12 (Brief, pages 11-12). Accordingly, pursuant to these statements and the provisions of 37 CFR § 1.192(c)(7)(1995), we select claims 1, 2 and 12 from the grouping and decide this appeal as to the ground of rejection on the basis of these claims alone. Illustrative claim 1 is reproduced and attached to this decision as an Appendix.

The examiner has relied upon the following references as evidence of obviousness:

Yamaguchi et al. (JP '833) 63-261833 Oct. 28, 1988
(Published Japanese Kokai Patent Application)[1]

Wolf et al. (Wolf), "Silicon Processing for the VLSI Era," *Vol. 1: Process Technology*, pp. 133-36, 303-08 and 321-22 (Sunset Beach, CA, Lattice Press, 1986).

The claims on appeal stand rejected under 35 U.S.C. § 103 as unpatentable over JP '833 in combination with Wolf (Answer, page 3). We *affirm* this rejection essentially for the reasons in the Answer and those reasons set forth below.

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[1]We rely upon and cite from a full English translation of this document previously made of record.

OPINION

The examiner finds that JP '833 discloses formation of a buried layer by implantation of either a p-type or n-type conductive impurity through an opening in a patterned layer followed by annealing and formation of an epitaxial layer on the substrate surface (Answer, page 3). The examiner further finds that JP '833 teaches an annealing temperature of 1000°C. (*Id.*, citing page 15 of the translation). The examiner finds that this reference fails to disclose or teach the temperature employed during epitaxial growth (Answer, page 4).

The examiner applies Wolf for the disclosure that epitaxial growth at temperatures equal to and above 1000°C. is conventional, as is the use of a photoresist layer or a patterned insulating layer as the implantation mask and annealing in a non-oxidizing atmosphere (Answer, pages 3 and 4). Furthermore, the examiner states that Wolf discloses full activation of implanted ions at temperatures of 800-1000°C., thus suggesting annealing at temperatures lower than 1000°C. (Answer, page 3). The examiner also concludes that the claims on appeal are construed as including any annealing temperature less than 1000°C., and such annealing temperatures would have been only a slight variation

from the disclosed annealing temperature of JP '833 with no expectation of materially altering the process (*Id.*).

Appellant argues that JP '833 is silent as to the annealing temperature (Brief, page 9) and that page 15 of the JP '833 translation does not disclose or imply annealing at 1000°C. (Reply Brief, page 2). Appellant's argument is not persuasive since JP '833, on page 15 of the translation, teaches that the maximum impure substance density should be up to the solubility of the p-type or n-type impure substance "based on the anneal temperature" used as shown in the annealing step of Part (3) in Figure 1. The reference immediately follows this statement with an example of the solubility of the common impurity boron in a silicon layer at 1000°C. This disclosure of JP '833 implies that annealing temperatures of 1000°C. are exemplary.

Appellant also argues that Wolf does not teach or suggest annealing and further heating at a temperature below 1000°C. followed by epitaxial growth beginning at a temperature of about 1000°C. (Brief, pages 10-11; Reply Brief, page 3). We disagree.

As found by the examiner (Answer, page 3), Wolf teaches that "full activation [of a boron impurity] is achieved at temperatures ~800-1000°C." (Wolf, page 305, ll. 1-2). Wolf subsequently teaches, with regard to annealing of crystalline

damage, that the higher the anneal temperature the better, within the range of 900-1000°C. (page 305, second full paragraph). This teaching, contrary to appellant's argument (Brief, page 11; Reply Brief, page 3), would not have led one of ordinary skill in the art away from using the claimed annealing temperatures, i.e., a temperature below 1000°C., since these temperatures include the upper limits of the range taught by Wolf. Furthermore, as stated by the examiner (Answer, page 3), temperatures slightly less than the temperature exemplified by JP '833 or the maximum of the range taught by Wolf would not have been expected to alter the process or product of JP '833. *See Titanium Metals Corp. of America v. Banner,* 778 F.2d 775, 783, 227 USPQ 773, 779 (Fed. Cir. 1985).

With regard to both annealing and epitaxial growth temperatures, Wolf teaches that these temperatures are result-effective variables. Wolf teaches that the net growth rate of epitaxial films depends on several parameters, one of which is deposition temperature (see page 135 and Figures 13 and 14). Wolf also teaches that full activation, achieved by annealing, is dependent on the dose of impurity used (page 305, ll. 2-3) as well as the rate of heating (page 307, last two paragraphs). It is well settled that the discovery of an optimum value of a

variable in a known process is normally *prima facie* obvious, absent any showing of unexpected results. *In re Boesch*, 617 F.2d 272, 276, 205 USPQ 215, 219 (CCPA 1980); *In re Antonie*, 559 F.2d 618, 620, 195 USPQ 6, 8-9 (CCPA 1977); *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955). We note that appellant has not submitted any evidence of unexpected results.

Appellant argues that "there is nothing . . . which would suggest to one skilled in the art that the process disclosed in the Japanese patent publication be revised in the manner proposed by the Examiner . . . . " (Brief, page 13). Appellant's argument is not well taken since, as discussed above, Wolf teaches the routine experimentation necessary to determine the optimum temperature for annealing and epitaxial growth in processes such as that taught by JP '833. Wolf not only suggests to those of ordinary skill in the art that they should carry out the claimed process but teaches a reasonable expectation of success. *In re Vaeck*, 947 F.2d 488, 493, 20 USPQ2d 1438, 1442 (Fed. Cir. 1991). See Wolf, pages 135-136, where Wolf teaches epitaxial growth deposition temperatures and suggests the expectation of success for values in the ranges taught (see also Figures 13 and 14, especially Region B in Figure 14). See also Wolf, pages 305, for the suggestion of temperatures required for

full activation of certain implanted ions (depending on the dose) and temperatures required to remove areas of crystalline damage. JP '833 discloses a process for annealing an ion-implanted region "to activate the impure substance" and to produce "excellent crystal characteristic[s] of the mono-crystal silicone epitaxially grown on the silicone substrate surface on the embedded [buried] layer." (Pages 7 and 13). Accordingly, Wolf would have suggested the modifications to the JP '833 process to one of ordinary skill in the art for reasons discussed above.

Appellant argues that the cited prior art does not disclose the subject matter recited in claim 2, namely transferring the substrate after ion implantation to a furnace for annealing and heating the substrate to expand the impurity region prior to growing the epitaxial layer (Brief, pages 11-12). Appellant also argues that the cited prior art does not disclose or suggest performing these steps in the same furnace, as specified by claim 12 (Brief, page 12).

Appellant's arguments are not persuasive. As noted by the examiner (Answer, page 4), Wolf teaches diffusion of the implanted impurities such that they expand the implanted region during the anneal process (see page 307, third full paragraph). Appellant has not responded to the examiner's contention that

some heating of the substrate is unavoidable after full activation or annealing of the implanted ions, thus leading to some expansion of the impurity region (Answer, page 4). On this record, we determine no reversible error in the examiner's position. We note that there is no lower limit recited in the claims on appeal as to the amount of "further heating" and subsequent expansion of the impurity region. We also note that JP '833 teaches ion implantation, annealing and epitaxial growth all in one furnace, with the epitaxial layer grown on the substrate layer before the impurity ion-implanted region has reached the surface of the substrate (page 9; Figure 1).

For the foregoing reasons, we determine that the examiner has established a *prima facie* case of obviousness in view of the reference evidence. Based on the totality of the record, giving due consideration to appellant's arguments, we determine that the preponderance of evidence weighs most heavily in favor of obviousness. Accordingly, we affirm the examiner's rejection of the claims on appeal under 35 U.S.C. § 103 as unpatentable over JP '833 combined with Wolf.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED

CHUNG K. PAK
Administrative Patent Judge

THOMAS A. WALTZ
Administrative Patent Judge

MICHAEL P. TIERNEY
Administrative Patent Judge

) BOARD OF PATENT APPEALS AND INTERFERENCES

TAW:hh

APPENDIX

1. A process for fabricating a semiconductor device comprising the steps of defining a window on the surface of a substrate where a buried impurity layer is to be formed, forming a resist on the surface of the substrate surrounding the window, implanting a p-type or n-type impurity ion into the substrate through the window, removing the resist, then annealing the substrate in a non-oxidizing atmosphere until the implanted impurity ions have been activated, thereafter further heating the substrate in a nonoxidizing atmosphere to expand the impurity ion-implanted region, both the annealing and the further heating steps being carried out at a temperature below 1000°C and below the epitaxial growth temperature, and gradually increasing the temperature up to a temperature of about 1000°C where epitaxial growth starts while preventing the impurity ion-implanted region from reaching the surface of the substrate so that a buried layer is formed, and subsequently, before the impurity ion-implanted region has expanded sufficiently to reach the surface of the substrate, growing an epitaxial layer on the surface of the substrate.

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Paper No. 23

Serial Number: 08/200,~~132~~ 312
Filing Date: 02/23/94
Appellant(s): Hidemi Takasu

Francis J. Hone
For Appellant

EXAMINER'S ANSWER

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This is in response to appellant's brief on appeal filed March 3, 1995.

(1) *Status of claims.*

The statement of the status of claims contained in the brief is correct.

(2) *Status of Amendments After Final.*

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

438/913 907

implant with (anneal or annealing)

with (epitaxy or epitaxial)

CUD

(3) *Summary of invention.*

The summary of invention contained in the brief is correct.

(4) *Issues.*

The appellant's statement of the issues in the brief is correct.

(5) *Grouping of claims.*

Appellant's brief includes a statement that claims 1,2 and 12 do not stand or fall together and provides reasons as set forth in 37 C.F.R. § 1.192(c)(5) and (c)(6).

(6) *Claims appealed.*

The copy of the appealed claims contained in the Appendix to the brief is correct.

(7) *Prior Art of record.*

The following is a listing of the prior art of record relied upon in the rejection of claims under appeal.

63-261833 Japan 10-1988

Wolf, S., et al., Silicon Processing for the VLSI Era: Vol.1, Process Technology, Lattice Press, pp.133-136, 303-308 and 321-322.

(8) *New prior art.*

No new prior art has been applied in this examiner's answer.

(9) *Grounds of rejection.*

The following ground(s) of rejection are applicable to the appealed claims.

Claims 1,2 and 10-12 are rejected under 35 U.S.C. § 103 as being unpatentable over Japanese Patent 63-261833 (Japan '833) taken in combination with Wolf et al.

Japan '833 discloses formation of a buried layer by implantation of either a p-type or an n-type conductive impurity through an opening in a patterned layer followed by annealing and formation of an epitaxial layer on the substrate surface. The use of a photoresist layer or a patterned insulating layer as the implantation mask is disclosed to be entirely conventional by Wolf et al, p.322. A partial translation of Japan '833 was obtained which indicates that the reference discloses annealing at 1000°C (p.157, lower left, and page 15 of the translation of Japan '833). It would have been within the scope of one of ordinary skill in the art to anneal at a temperature slightly below 1000°C, a slight variation from this temperature not being expected to materially alter the process. This would by expected to merely increase the processing time slightly. Note that Wolf et al discloses full activation of implanted ions at temperatures of 800-1000°C, thus reinforcing the suggestion to vary the anneal temperature slightly from the 1000°C disclosed by Japan '833 (Wolf et al, pages 303-308). The claims are open to any temperature less than 1000°C in the anneal step. The reference does not appear to

anneal in an oxidizing atmosphere, and thus discloses annealing in a non-oxidizing atmosphere, because oxide formation and removal prior to epitaxial growth are not depicted. If annealing in a non-oxidizing atmosphere is not disclosed, to do so would have been within the scope of one of ordinary skill in the art as discussed by Wolf et al, pp.303-308, especially p.305, third full paragraph. Heating of the substrate for some time period after the anneal step is in practice unavoidable when desiring to fully activate the implanted ions, i.e. how does one stop the anneal at the exact moment of achieving "annealing" of the substrate? Diffusion of the implanted impurities to expand the implanted region necessarily takes place during the anneal (Wolf, et al, p.307, third full paragraph. The reference does not disclose the epitaxial growth temperature. Wolf et al discloses epitaxial growth at temperatures equal to and above 1000°C to be conventional (p.136, fig.14). It therefor would have been within the scope of one of ordinary skill in the art to perform the epitaxial growth step of Japan '833 at the temperatures equal to and above 1000°C shown to be suitable by Wolf et al. To use a separate furnace for 1)the implantation and 2)the annealing, diffusion and epitaxial growth steps requiring transfer of the wafer as in claim 2, is well within the scope of one of ordinary skill in the art, the effects of exposure of the wafer to the ambient air being well known, such as surface contamination. It also would have been within the scope of one of ordinary skill in the art to perform the epitaxial growth without cooling the wafer after annealing and diffusion of the implanted ions because cooling of the wafer is not disclosed as necessary by Japan '833 and because the epitaxial growth temperature is higher than the annealing and

diffusion temperature, i.e. a further process step entailing increased processing time and energy consumption is required to cool the wafer.

(11) *Response to argument.*

Applicant's arguments have been addressed in the statement of the rejection above.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

George Fourson
Primary Examiner
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GeorgeFourson
December 13, 1995

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